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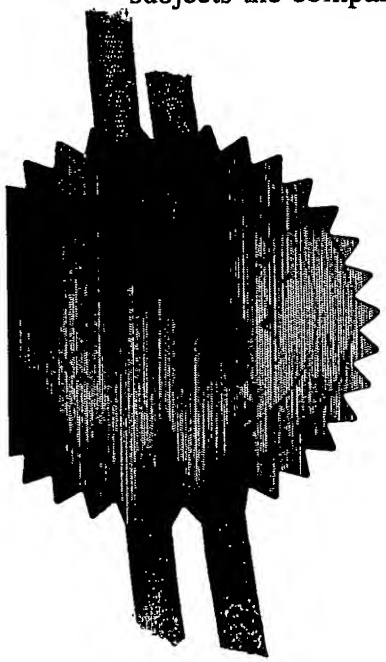

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1. Your reference — SP/4131 GB

2. Patent application number *(The Patent Office will fill in this part)* — 0316082.7 — 0 9 JUL 2003

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
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Patents ADP number *(if you know it)* 8254088001

If the applicant is a corporate body, give the country/state of its incorporation — UNITED KINGDOM

4. Title of the invention — METHOD OF FABRICATING AN ELECTRON MULTIPLIER ARRAY

5. Name of your agent *(if you have one)* — STEVENS HEWLETT & PERKINS

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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STEVENS HEWLETT & PERKINS

12. Name and daytime telephone number of person to contact in the United Kingdom: SARAH PERKINS 020 7404 1955

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# METHOD OF FABRICATING AN ELECTRON MULTIPLIER ARRAY

The present invention relates to a method of fabricating an electron multiplier array and to an electron multiplier array made by this method. In particular, the invention is concerned with the fabrication of an array of discrete-dynode electron multipliers suitable for, but not limited to, use in microchannel plates, photomultipliers and ion detectors.

A discrete-dynode electron multiplier generally comprises a plurality of dynodes arranged in a stack with each dynode physically and electrically isolated from its neighbours by an insulator and with each dynode including a material having high secondary electron emission characteristics and having an applied voltage related to the position of the dynode in the stack. A conventional manufacturing method for a discrete-dynode electron multiplier array consists of the alternate stacking of separately fabricated dynode layers and insulation layers with each layer including a plurality of apertures that during stacking are positioned to align with apertures in adjacent layers so as to form a plurality of multiplier channels.

EP 0515261 describes an electron multiplier array formed by stacking a plurality of ceramic plates that are subsequently baked. Prior to stacking, apertures are formed in each of the ceramic plates by mechanical punching or drilling and some of the plates have their apertures lined with a conductive coating. Some or all of the plates that are lined with a conductive coating are also provided with a conductor that connects the conductive coating to an electrical contact provided on the side of the plate. The conductive coating is also treated to improve its secondary electron emissivity. The plates are then stacked to form alternate dynode and insulation layers. Each dynode layer comprises one or more plates having conductive coatings to which an electrical potential is applied by means of the electrical contact. Each insulation layer consists of one or more plates having no conductive coatings. The apertures mechanically machined into the plates making up the insulation layers are smaller than those making up

the dynode layers such that the resulting stacked structure comprises a plurality of varying diameter, cylindrical channels.

Electron multiplier arrays of the type described in EP 0515261 suffer from the disadvantage that the channels are relatively large and are susceptible to high magnetic fields which significantly reduces the potential applications for such devices.

WO 97/05640 describes the manufacture of a discrete-dynode electron multiplier array through the use of micromachining and thin film techniques. The method described in this document consists of forming silicon dioxide layers on the opposed upper and lower faces of a silicon wafer and then enclosing the silicon wafer and the silicon dioxide layers with an outer layer of silicon nitride. An upper surface of the silicon nitride is coated with a photoresist in which apertures are lithographically formed. The apertures in the photoresist are then extended by reactive ion etching through the silicon nitride and the silicon dioxide immediately below before wet chemical etching is used to form tapered apertures in the silicon wafer. The photoresist is removed and the nitride layer immediately beneath the photoresist is removed by dry etching. A HF wet etch is then used to remove the silicon dioxide layer over the upper surface of the silicon wafer, exposed by the removal of the silicon nitride layer, as well as those regions of the lower layer of silicon dioxide exposed at the bases of each of the tapered apertures. Hot phosphoric acid is then used to remove the remaining silicon nitride leave a preform consisting of a silicon wafer with a layer of silicon dioxide having a plurality of through apertures tapering from the silicon wafer towards the silicon dioxide layer. Pairs of performs are then bonded face-to-face (i.e. silicon-to-silicon) to form discrete dynode elements and a plurality of these discrete dynode elements are then stacked (silicon dioxide-to-silicon dioxide) with their through apertures aligned to form continuous channels. Finally, an electron-emissive film is deposited on the exposed tapered silicon surfaces in each of the channels to form an array of electron multipliers.

Although WO 97/05640 describes the manufacture of a much smaller multiplier array than that described in EP 0515261, the document describes only the use of silicon as the dynode layer with wet chemical etching being used to form the apertures in the silicon.

Whilst deep reactive ion etching is also known for etching tapered apertures, the process is expensive and requires precise control of parameters such as etchant and passivation gases, process pressures, switching ratios, coil and platen powers.

EP 1004134 also describes an electron multiplier array comprising a stack of metallic dynode layers and insulator layers alternately deposited on a substrate. Apertures are etched through each of the layers in turn to form an array of channels and the exposed surfaces of the dynodes in each channel are coated in a material having a high secondary emission coefficient. Whilst this method permits the fabrication of small devices, fabrication is limited to materials that can be deposited and etched and the apertures formed in each of the dynode layers are not tapered.

It is an object of this invention to provide an alternative method of manufacture of an electron multiplier array that is capable of forming tapered dynode apertures. In having dynode apertures with tapered rather than vertical walls, the probability of an electron striking the dynode as it travels through the channels of the electron multiplier array is increased.

Accordingly, in a first aspect the present invention provides a method of manufacturing an electron multiplier array comprising the steps of: providing an electrical insulation layer having a first surface and an opposing second surface; applying a dynode layer to the first surface of the insulation layer; applying a protective layer to the second surface of the insulation layer; ablating one or more apertures through at least the dynode layer and the insulation layer by means of a jet of powder particles; etching those surfaces of the insulation layer exposed by the apertures; removing the protective layer to create a discrete block; and stacking and aligning a plurality of said discrete blocks to create a stack, wherein the apertures in

the discrete blocks align to form a plurality of channels extending through the stack.

The dynode layer is preferably formed of an electrically conductive material, which may have a high secondary-electron emission coefficient. Where the dynode layer comprises a material having a low secondary-electron emission coefficient, the method further comprises the step of coating the walls of the apertures formed in the dynode layer with a high secondary-electron emissive material.

Whilst the dynode layer is preferably formed of an electrically conductive material, the dynode layer may instead be formed of an electrical insulator. The method then further comprises the step of providing electrical connections on the surface of the dynode layer remote from the insulation layer for applying a voltage potential to the coatings of a high secondary-electron emissive material.

The dynode layer and the electrical insulation layer are preferably thermally matched to prevent deformation or separation of the layers that might arise during the subsequent operation of the multiplier array.

The ablation of one or more apertures is preferably carried out by applying a masking having through-apertures to either the surface of the dynode layer remote from the insulation layer or the surface of the protective layer remote from the insulation layer, and rastering the jet of hard powders over the mask.

The method preferably includes providing each discrete block with one or more alignment keys, which are subsequently used to align the plurality of stacked blocks. In particular, the blocks may be aligned by aligning at least one alignment key of each discrete block with at least one alignment key of an adjacent discrete block.

In a second aspect, the present invention provides an electron multiplier array comprising a plurality of alternately stacked layers of a dynode material and an electrical insulator, each stacked layer having a plurality of apertures which align with apertures in adjacent layers to form

an array of open channels extending through the stacked layers, wherein the walls of the apertures in each dynode layer are tapered and a portion of the upper and lower surfaces of each dynode layer surrounding the apertures is exposed.

The apertures in each layer of dynode material are preferably positioned so as to only partially overlap the apertures in the preceding layer of dynode material. Moreover, the positions of the apertures in the stacked layers are preferably arranged such that each channel of the array describes a repeating S-shaped path.

The stacked layers may be mounted on a substrate that closes one end of the channels of the array, with an anode is preferably provided at the closed end of the channel.

Thus with the present invention a method of manufacture of an electron multiplier array is provided which enables a discrete-dynode electron multiplier array to be formed with tapered aperture walls in a particularly cost-effective manner. Moreover, electron multiplier arrays having large surface areas, e.g. greater than a metre square, may be manufactured, or electron multiplier arrays may be formed from a single substrate or discrete block from which segments are subsequently cut and then stacked.

An embodiment of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a schematic cross sectional view of a single channel of an electron multiplier array in accordance with a first embodiment of the present invention;

Figure 2 is a schematic cross sectional view of a single channel of an electron multiplier array in accordance with a second embodiment of the present invention;

Figure 3 illustrates a step in the process of manufacturing the electron multiplier array of Figure 1;

Figure 4 illustrates a further step in the process of manufacturing the electron multiplier array of Figure 1;

Figure 5 illustrates a further step in the process of manufacturing the electron multiplier array of Figure 1; and

Figure 6 illustrates a further step in the process of manufacturing the electron multiplier array of Figure 1.

The electron multiplier array 1 illustrated in Figure 1 comprises a stack of blocks a,b,c each block consisting of a pair of layers, one of the pair being a dynode layer 2 and the other of the pair an insulation layer 3. The blocks a,b,c are stacked such that the dynode layers 2a,2b,2c and the insulation layers 3a,3b,3c alternate through the stack. In addition, each layer 2,3 of the multiplier array 1 has a plurality of through apertures which are in communication with the apertures in adjacent layers so as to define an array of continuous channels 8 extending through the stack from an upper surface 4 to a lower surface 5 of the electron multiplier array 1.

The channels 8 of the electron multiplier array 1 are preferably arranged in a regular grid formation with a spacing of between 10 and 500 microns, preferably less than 100 microns.

The apertures in each dynode layer 2 are tapered towards the lower surface 5 of the electron multiplier array 1 such that the diameter of the aperture at the upper surface 6 of the dynode layer 2 is greater than that at the lower surface 7. Tapering of the aperture walls in this manner ensures that electrons travelling through the channels 8 of the electron multiplier array 1 will strike the dynode layers 2 with a greater probability than that if the aperture walls had been vertical.

The shape of the aperture at the upper surface of each dynode layer 2 is preferably circular. However, as is described below, alternate shapes are possible. Each aperture in the dynode layer 2 preferably has a diameter of around 100 microns. However, apertures of diameters between 50 and 1000 microns are also envisaged. The axes of the apertures in each dynode layer 2 are partially offset with respect to the

axes of the apertures in adjacent dynode layers such that the walls of the apertures in each dynode layer partially overlie apertures in the dynode layer immediately below. Ideally, the axes of the apertures in the dynode layers 2a,2b,2c are arranged such that each channel 8 describes a repeating S-shaped path.

As illustrated, the size of the apertures in the insulation layers 3a,3b,3c are greater than the dynode aperture size. Each aperture in the insulation layer 3 preferably has a diameter of around 120 microns, though again apertures of diameters between 60 and 1100 microns are also envisaged. Thus, the apertures in each insulation layer 3 are sized so as to expose upper 38 and lower 39 surface edge regions of each dynode layer 2. The exposed upper 38 and lower 39 surface edge regions ensure that, when an electron impacts the dynode layer 2, charge leakage across the dynode layer 2 is reduced.

Each dynode layer 2 is formed of a material that can be etched by powder blasting techniques. Preferably, each dynode layer 2 is formed of a thermally-conductive and electrically-conductive material and in particular a fired electrically-conductive ceramic such as high density graphite or pyrolytic carbon. Alternative electrically-conductive pressed ceramics may also be used, but graphite materials are preferred due to their high thermal conductivity and resistance to hydrofluoric acid and phosphoric acid etchants. Other suitable electrically-conductive materials include rutile, doped alumina, doped zirconia or crystalline molybdenum. Alternatively, each dynode layer 2 may be formed of an electrical insulator, in particular an electrical insulating ceramic. Where the dynode layer 2 is an electrical insulator, tracks of an electrically conductive material are provided on a surface of the dynode layer 2. The tracks are preferably in a regular grid formation having a dynode aperture at each node of the grid and preferably extend into and cover at least a region of the aperture walls of the dynode layer 2.

A thin layer of high secondary-electron emissive material 41 (having a secondary-electron emission coefficient of at least 5) lines the walls of the apertures in each dynode layer 2. Suitable materials include, but are not limited to, lithium fluoride, sodium fluoride, sodium chloride, potassium chloride, rubidium chloride, caesium chloride, sodium bromide, potassium iodide, caesium dioxide and caesiated antimony. The exposed upper surface edge regions 38 of each dynode layer 2 may additionally be coated with the high secondary-electron emissive material. The thickness of the coating 41 of high secondary-electron emissive material is preferably between 10nm and 200nm.

Each dynode layer 2 may be formed of a material that is both electrically conductive and has a high secondary-electron emission coefficient, e.g. carbon doped with antimony or caesium. The coatings 41 of high secondary-electron emissive material may therefore be omitted.

Each dynode layer 2 is also provided with an electrical connection (not illustrated) such that a voltage potential may be applied either to the dynode layer 2 or, where the dynode layer 2 is formed of an electrical insulator, to the tracks provided on the surface of the dynode layer 11. Any voltage potential applied to the electrical connection is consequently applied to the coatings 41 of emissive material that line the aperture walls of each dynode layer 2. The level of the applied voltage potential is dependent upon the position of the dynode layer 2 in the stack.

Each insulation layer 3 is made preferably of aluminium oxide or silicon dioxide. However, as is described below, other electrically insulating materials, such as polyimides and polyamides, may alternatively be employed as long as they can be selectively etched with respect to the dynode material and are substantially thermally matched with the dynode material. For example, Corning® 7740 may be used for the insulation layers 3 in conjunction with crystalline molybdenum for the dynode layers 2, and aluminium oxide may be used for the insulation layers 2 in conjunction with high density graphite. By thermally matching the materials of the

dynode 2 and insulation 3 layers, the risks of distortion and damage through unequal thermal expansion, such as might occur during baking of the structure or during operation of the electron multiplier array 1, is reduced.

As illustrated in Figure 1, each channel 8 of the electron multiplier array 1 is open at both ends. In this embodiment it is envisaged that the electron multiplier array 1 be used, for example, as a microchannel plate. Nevertheless, it will be appreciated that other implementations of the electron multiplier array are possible. In particular, Figure 2 illustrates an implementation of the electron multiplier array 1 for use as an ion or photon detector. The electron multiplier array 1 is mounted on a substrate 30 and respective anodes 36 are disposed at one end of each channel 8 of the array 1. Each anode comprises a thin metal film 32 having a low secondary-electron emission coefficient deposited over a convex-shaped element 31 and has an electrical connection 33 in the form of a thin metal strip. The thin metal film 32 preferably comprises a chromium:gold alloy and has a thickness of between 0.05 and 4 microns, more preferably between 0.1 and 1 microns. The electrical connections 33 are preferably formed of the same metallic material.

A conversion electrode 34, such as a photocathode, is provided on the upper surface 4 of the electron multiplier array 1 and consists of, for example in the case of a photodetector or image intensifier, a layer of a photosensitive material applied to the exposed upper surface 38 of the uppermost dynode. Alternatively, the conversion electrode may be mounted above but separate from the apertures of the electron multiplier array. With the multiplier array illustrated in Figure 2, the array 1, anodes 36 and conversion electrode 34 are sealed in a high-vacuum package with a quartz or glass window 35 aligned with the openings to the channels 8.

The method of manufacturing the electron multiplier array 1 of Figures 1 and 2 will now be described with reference to Figures 3-5.

A dynode layer 11 having opposed first 15 and second 16 surfaces, has a layer of electrically insulating material 12 attached to its first surface 15. Both layers are substantially thermally matched (i.e. have similar thermal expansivities) to prevent deformation or separation of the layers during a later step of baking as well as during operation of the multiplier array 1. The dynode layer is 11 is preferably formed of high density graphite whilst the insulation layer 12 is preferably formed of aluminium oxide. Other materials suitable for the dynode layer 11 and insulation layer 12 are provided both above and below.

The dynode layer 11 and the insulation layer 12 are preferably wafers adhered by conventional wafer-level bonding, e.g. adhesive applied by spin or spray coating or by bubble-jet printing. However, in the alternative the insulation layer 12 may be secured to the dynode layer 11 for example by spin coating spin-on-glass or sol gel. The insulation layer 12 may also be applied by vacuum techniques that allow for anodic bonding, especially where the dynode layer is formed of electrically-conductive silicon and the insulation layer is formed of a glass that can be anodically bonded to silicon, e.g. CMZ or Corning® 7740 glass.

The thickness of the dynode layer 11 is ideally substantially similar to the thickness of the insulation layer 12 and preferably has a thickness of between 30-200 microns, ideally around 50 microns. Ultimately, however, the thickness of each layer is a matter of design preference and may depend upon the desired characteristics of the electron multiplier array 1, as well as the choice of materials for the dynode layer 11 and insulation layer 12.

The dynode 11 and insulator 12 layers are mounted on a carrier or handler 14, such as a stainless steel disc, for ease of handling during the subsequent manufacturing stages. The carrier is preferably rigid and is resistant to the chemical etchants that are employed in the subsequent manufacturing steps. The dynode 11 and insulation layers 12 are preferably adhered to the carrier 14 by means of a water-soluble adhesive.

However, other means for mounting the layers on the carrier 14, e.g. clamping, may be employed. It will be appreciated that the carrier 14 is not essential to the fabrication of the electron multiplier array 1 and that the carrier 14 may in fact be omitted from the manufacturing process.

A protective layer 13 is then applied to the exposed surface 17 of the insulation layer 12. The protective layer 13 is preferably a thin film of chromium applied by conventional deposition techniques over the surface 17 of the insulation layer 12 opposite the dynode layer 11. As is described below, the protective layer 13 serves to protect the surface 17 of the insulation layer 12 during selective etching of the insulation layer 12 and to maintain the thickness of the insulation layer 12 during the etching process. Accordingly, the protective layer 13 may consist of any material that is resistant to the chemical etchant used to etch the insulation layer 12, including metals and polymers. For example, aluminium may be used as an alternative to chromium when hydrofluoric acid is used to etch the insulation layer 12. The thickness of the thin film is chosen to be sufficiently thick to provide adequate protection during the etching process, but not overly thick so that the protective layer 13 may subsequently be removed reasonably quickly. For most suitable materials, a thickness of between 0.1 to 1.0 microns is appropriate.

It will be appreciated that the order of the process steps described above is not particularly significant. For example, the initial fabrication steps may comprise the provision of the insulation layer 12 to which is applied the protective layer 13. The dynode layer 11 may then be secured to the insulation layer 12 before the construct 20 of dynode layer 11, insulation layer 12 and protective layer 13 is mounted on the carrier 14.

A photoresist mask 19 is applied to the exposed second surface 16 of the dynode layer 11. The mask 19 preferably comprises a photosensitive emulsion such as rubber. However, alternative masks that can be defined lithographically and can withstand a powder blasting process may alternatively be used. The mask 19 is patterned by optical

lithography, e.g. UV light, to define one or more apertures in the mask 19. Of course other forms of lithography may be employed. The apertures defined in the mask 19 are preferably circular in shape and have a diameter of between 50 microns and 1000 microns, ideally around 100 microns. Moreover, the apertures are preferably arranged in regular grid formation with a spacing of between 10 and 2000 microns, and preferably less than 200 microns. Other shapes, sizes and distribution of apertures may of course be defined in the mask 19 as desired.

Although the mask 19 is preferably a photoresist, other masks that can withstand the powder blasting process and which can be removed without damage to the dynode 11 or insulation layer 12 may also used. In particular, metal masks formed of, for example, nickel or copper may be formed on the exposed second surface 16 of the dynode layer 11 by electroplating. Alternatively, the mask 19 may comprise a metal grid formed of, for example, nickel or stainless steel that is bonded to the exposed second surface 16 of the dynode layer 11.

The regions 21 of the second surface 16 of the dynode layer 11 exposed by the apertures in the mask 19 are then subjected to powder blasting, or abrasive jet machining. A particle jet 22 of hard powders, such as silicon carbide and/or aluminium oxide, is rastered over the second surface 16 of the dynode layer 11 at an angle substantially normal to the upper surface 16. Naturally, the material used for the hard powder must be harder than those materials used for the dynode layer 11 and insulation layer 12. For example, aluminium oxide may be used for the hard powder when the insulation layer 12 is made of silicon dioxide, whilst silicon carbide (which is harder than aluminium oxide) may be used when the insulation layer 12 is made of aluminium oxide. The average particle size of the powder is preferably between 5 microns and 20 microns. The particle jet 22 ablates through the regions 21 of the dynode layer 11 exposed by the apertures in the mask 19 to produce tapered apertures through at least the dynode layer 11 and the insulation layer 12. The

particle jet 22 also preferably ablates through the protective layer 13. The pressure at the nozzle is preferably between 30-100 psi (0.2-0.7 MPa) and the distance between the dynode layer 11 and the nozzle is preferably around 10cm. By employing these parameters, apertures having tapered walls of between 20° and 45° from the normal are formed for layers of high-density graphite and aluminium oxide. However, tapering of the apertures may be made more acute or obtuse by varying, among other things, the material of the dynode layer 11, the abrading powder, the pressure and collimation of the jet 22, the mask thickness and the separation of the dynode layer 11 and nozzle. Moreover, asymmetrical tapering may be achieved by varying the angle of incidence of the jet 22 relative to the second surface 16 of the dynode layer 11.

Whilst in the above embodiment, the mask 19 is applied to the second surface 16 of the dynode layer 11, the mask may alternatively be applied the surface of the protective layer 13 remote from the insulation layer 12. The particle jet 22 then ablates through the regions of the protective layer 13 exposed by the apertures in the mask 19 to produce tapered apertures in the protective layer 13, the insulating layer 12 and the dynode layer 11. In the preferred embodiment, in which the mask 19 is applied to the surface 16 of the dynode layer 11, the insulation layer 12 is adjacent that surface of the dynode layer 11 for which the aperture diameters are smallest, i.e. the insulation layer 12 is disposed below the dynode layer 11 of the discrete block 40 (see Figure 5). However, when the mask 19 is applied to the surface of the protective layer 13, the insulation layer 12 is adjacent that surface of the dynode layer 11 for which the aperture diameters are greatest, i.e. the insulation layer 12 is disposed above the dynode layer 11 of the discrete block 40.

The mask 19 is subsequently removed from the dynode layer 11, preferably by placing the construct 20 (dynode layer 11, insulation layer 12 and protective layer 13) mounted on the carrier 14 in a bath of mask stripper (hot water and stencil remover concentrate in the case of

elastomer masks). Other solutions known to selectively remove photoresist masks may alternatively be used, e.g. piranha solution. The solution used to remove the mask 19 will naturally depend upon the mask material. When the mask 19 comprises an electroplated metal mask, the mask 19 may instead be removed at a later stage along with the protective layer 13.

The tapered walls 23 of the apertures through the insulation layer 12 are thereafter selectively etched by placing the construct 20 and carrier 14 in a bath of phosphoric acid. The protective layer 13 prevents etching at the surface 17 of the insulation layer 12 and ensures that etching occurs only at the aperture walls 23 formed by the powder blasting process. The protective layer 13 prevents etching at the otherwise exposed surface 17 of the insulation layer 12 such that the thickness of the insulation layer 12 is maintained. As a result of the etching process, the size of the apertures in the insulation layer 12 is increased such that the diameter of the apertures in the insulation layer 12 adjacent the join with the dynode layer 11 is greater than the diameter of the apertures in the dynode layer 11 at the join. When an electron strikes the dynode layer 11, the regions 37 of the first surface 15 of the dynode layer 11 exposed by etching the insulation layer 12 assist in reducing charge leakage across the dynode layer 11. Each aperture in the insulation layer 12 preferably has an average diameter of around 110 microns, though average diameters of between 60 and 1010 microns are also envisaged. The chemical etchant and material used for the protective layer 13 are chosen such that etching of the construct 20 occurs only at the aperture walls 23 of the insulation layer 12. The choice of chemical etchant and protective material will depend upon the materials selected for the dynode layer 11 and insulation layer 12. Possible combinations are provided by way of example in the table below:

| Dynode Layer | Insulation Layer | Protective Layer | Chemical Etchant |
|---|---|---|---|
| GaP, CsSb, C-Sb | Glass | Polysilicon, Cr, Al, Black wax, BCB | Hydrofluoric Acid |
| High density graphite | Aluminium Oxide | Polyimide, Black Wax | Phosphoric Acid |

The protective layer 13 is subsequently removed from the surface 17 of the insulation layer 12 to produce a block 40 mounted on the carrier 14. Referring to Figure 5, the block 40 consists of two layers: a dynode layer 11 and an insulation layer 12 having a plurality of through apertures. Where the protective layer 13 comprises a thin film of chromium, a wet chemical etch of alkaline hexacyanoferrate(III)-solution may be employed to remove the protective layer 13. The selection of chemical etchant naturally depends upon the choice of materials for the dynode layer 11, insulation layer 12 and protective layer 13. For example, phosphoric acid may be used to remove a thin film of aluminium, which may be used as the protective layer 13 when the insulation layer 12 is made of glass and hydrofluoric acid is used to etch the insulation layer 12.

The aperture walls of the dynode layer 11 are then coated, using thermal or electron beam evaporation or ion beam sputtering, with a thin layer of material having a high secondary-electron emission coefficient, i.e. a coefficient of at least 5. Suitable materials have been described above. The thickness of the high secondary-electron emissive material is preferably between 10nm and 200nm.

Although the dynode apertures are coated with a high secondary-electron emissive material preferably prior to stacking the blocks (as described below), the high secondary-electron emissive material may alternatively be deposited over the aperture walls of the dynode layers 11 after the blocks have been stacked and baked.

When the dynode layer 11 is formed of an electrical insulator, tracks of a thin metallic material are deposited onto the second surface 16 of the dynode layer 11 prior the aperture walls being coated with the high secondary-electron emissive material. The pattern of the tracks and the width of each track are chosen such that (i) the tracks interconnect all apertures in the dynode layer 11 and (2) a sufficient fraction of the second surface 16 of the dynode layer 11 is available for thermally bonding to an insulation layer 12 during the subsequent step of baking, as described below. The tracks are preferably formed in a regular grid formation having a dynode aperture at each node of the grid, and each track preferably has a width of around 50 nm. The tracks preferably extend into and cover at least a region of the aperture walls of the dynode layer 11. Indeed, the material used to form the tracks may be deposited over the entire surface of the dynode aperture walls. The material used to form the tracks preferably has a low electrical resistance (less than 0.01 Ohm-cm). The tracks serve as electrical connections for applying a voltage potential to the coatings of high secondary-electron emissive material that line the aperture walls of the dynode layer 11. Naturally, when the dynode layer is electrically conductive, voltage potentials may be applied directly to the dynode layer 11.

When the dynode layer 11 comprises a material that is both electrically conductive and has a high secondary-electron emission coefficient, e.g. carbon doped with antimony or caesium, the step of coating the aperture walls of the dynode layer 11 with a high secondary-electron emissive material may be omitted.

The carrier 14 is then removed from the block 40. When a water-soluble adhesive is employed as the preferred means for securing the dynode 11 and insulation layers 12 to the carrier 14, the carrier 14 can be separated from the block 40 by placing them in a bath of water.

The surface area of the block 40 is preferably a multiple of the required surface area of the electron multiplier array 1. The block 40 is

then sliced into smaller substantially identical segments 24 which are stacked one on top of the other with the dynode layers and the insulation layers alternating. The segments 24 are stacked such that the apertures form continuous channels through all segments of the stack. However, each segment 24 is preferably positioned such that the apertures are partially off-set with respect to the apertures in the neighbouring segments in the stack. In this way the channels are caused to describe a non-linear path, preferably a repeating S-shaped path. Once the stack is complete it is then baked at between 150-500°C for 1 hour under vacuum, for example, to thermally bond the individual segments together to form the electron multiplier array 1 illustrated in Figure 1. The dynode layers 11 of the stacked segments serve as the discrete dynode layers 2 of the electron multiplier array 1, whilst the insulation layers 12 serve as the insulation layers 3.

In order to aid the accurate alignment of the segments 24 within the stack, each segment 24 is preferably provided with an alignment key. The alignment key may comprise an additional aperture formed in each segment 24 that are required to be aligned. Alternatively, the mask 19 and protective layer 13 may be patterned such that one or more notches, e.g. V-shaped notch, are formed on opposing surfaces of each segment 24. It will of course be apparent that other forms of alignment key conventionally employed in wafer alignment may alternatively be used.

Finally, the dynode layer 11 of each segment 24 (i.e. each dynode layer 2) is provided with an electrical connection such that a voltage potential may be applied either to the dynode layer 11 or, where the dynode layer 11 comprises an electrical insulating material, the tracks provided on the second surface 16 of the dynode layer 11.

In fabricating the embodiment illustrated in Figure 2, an array of convex-shaped elements 31 are separately lithographically defined on a substrate 30 such as a silicon wafer (only one convex-shaped element 31 is illustrated in Figure 2). The convex-shaped elements 31 are preferably

of a thermally deformable plastics which adopt a generally convex shape following exposure to heat. A thin metal film 32 having a low secondary-electron emission coefficient is then deposited over the surfaces of the convex-shaped elements 31 and the exposed surface of the substrate 30. The thin metal film 32 preferably comprises an chromium:gold alloy and has a thickness between 0.05 and 4 microns in thickness, more preferably between 0.1 and 1 microns. The thin metal film 32 is then patterned using conventional etching techniques to leave the surface of each convex-shaped element 31 covered by the thin film 32 to form an array of anodes 36. Each anode 36 also has an electrical connection 33 in the form of a thin metal strip. The segments 24 are then stacked on the substrate 30 and arranged such that each channel 8 through the stack has a respective anode 36 disposed at one end.

The conversion electrode 34 is preferably formed by applying a coating of a photosensitive material, for example, to regions of the uppermost surface of the stack immediately adjacent each channel 8. Finally, electrical connections are made to each anode and each dynode layer 2 and the entire structure is sealed inside a steel or glass package under vacuum.

The electron multiplier array is intended to be suitable for use in, among other things, photomultipliers, charged particle detectors, large-area flat panel displays and secondary-electron emission microscopy.

By means of the powder blasting manufacturing method described herein, a simple and cost effective method of fabricating electron multiplier arrays is provided. In particular, a substrate having a large surface area (a metre square or more) may have many apertures formed in it by rastering a jet of powders over the surface of the substrate in a particularly cost-effective manner. This additionally enables electron multiplier arrays to be formed from a single flat substrate from which segments are subsequently cut and then stacked.

## CLAIMS

1. A method of manufacturing an electron multiplier array comprising the steps of:

providing an electrical insulation layer having a first surface and an opposing second surface;

applying a dynode layer to the first surface of the insulation layer;

applying a protective layer to the second surface of the insulation layer;

ablating one or more apertures through at least the dynode layer and the insulation layer by means of a jet of powder particles;

etching those surfaces of the insulation layer exposed by the apertures;

removing the protective layer to create a discrete block; and

stacking and aligning a plurality of said discrete blocks to create a stack, wherein the apertures in the discrete blocks align to form a plurality of channels extending through the stack.

2. A method as claimed in claim 1 further comprising the step of coating the walls of the apertures formed in the dynode layer with a material having a secondary-electron emission coefficient of at least 5.

3. A method as claimed in claim 2 further comprising the step of providing electrical connections on the surface of the dynode layer remote from the insulation layer for applying a voltage potential to the coatings of a high secondary-electron emissive material.

4. A method as claimed in either of claims 1 or 2, wherein the dynode layer comprises a material that is electrically conductive.

5. A method as claimed in any one of the preceding claims further comprising the step of providing a mask having one or more through apertures on the surface of the dynode layer remote from the insulation layer, and the step of ablating one or more apertures through at least the dynode layer and the insulation layer comprises rastering the jet of particle powders over the mask.

6. A method as claimed in any one claims 1 to 4 further comprising the step of providing a mask having one or more through apertures on the surface of the protective layer remote from the insulation layer, and the step of ablating one or more apertures through at least the dynode layer and the insulation layer comprises rastering the jet of particle powders over the mask.

7. A method as claimed in any one of the preceding claims further comprising the step of providing each discrete block with one or more alignment keys and the step of aligning a plurality of said discrete blocks comprises aligning at least one alignment key of a discrete block with at least one alignment key of an adjacent discrete block.

8. A method as claimed in any one of the preceding claims wherein each discrete block has a surface area of at least 1 square metre.

9. A method as claimed in any one of the preceding claims further comprising the step of cutting the discrete block into discrete segments and wherein the steps of stacking and aligning a plurality of said discrete blocks comprises stacking and aligning a plurality of said discrete segments to create a stack, wherein the apertures in the discrete segments align to form a plurality of channels extending through the stack.

10. A method as claimed in any one of the preceding claims, wherein the dynode layer and electrical insulation layer are thermally matched.

11. An electron multiplier array comprising a plurality of alternately stacked layers of a dynode material and an electrical insulator, each stacked layer having a plurality of apertures which align with apertures in adjacent layers to form an array of open channels extending through the stacked layers, wherein the walls of the apertures in each layer of dynode material are tapered and a portion of the upper and lower surfaces of each layer of dynode material surrounding the apertures is exposed.

12. An electron multiplier array as claimed in 11, wherein the dynode material has a secondary-electron emission coefficient of at least 5.

13. An electron multiplier array as claimed in 11, wherein the walls of the apertures in each layer of dynode material are coated with a material having a secondary-electron emission coefficient of at least 5.

14. An electron multiplier array as claimed in 13, wherein each layer of dynode material has a respective electrical connection to the coatings of high secondary-electron emissive material for application of a voltage potential to the coatings.

15. An electron multiplier array as claimed in any one of claims 11 to 13, wherein the dynode material is electrically conductive.

16. An electron multiplier array as claimed in any one of claims 11 to 15, wherein the layers of dynode material and the layers of electrical insulator are thermally matched.

17. An electron multiplier array as claimed in any one of claims 11 to 16, wherein the dynode material is non-metallic.

18. An electron multiplier array as claimed in any one of claims 11 to 17, wherein the apertures in each layer of dynode material are positioned so as to only partially overlap the apertures in the preceding layer of dynode material.

19. An electron multiplier array as claimed in any one of claims 11 to 18, wherein the positions of the apertures in the stacked layers are arranged such that each channel of the array describes a repeating S-shaped path.

20. An electron multiplier array as claimed in any one of claims 11 to 19, wherein the plurality of alternately stacked layers are mounted on a substrate that closes one end of the channels of the array.

21. An electron multiplier array as claimed in claim 20, wherein an anode is provided at the closed end of each channel of the array.

22. An electron multiplier array as claimed in claim 21, wherein each anode comprises a convex-shaped element over which is deposited a thin metallic film.

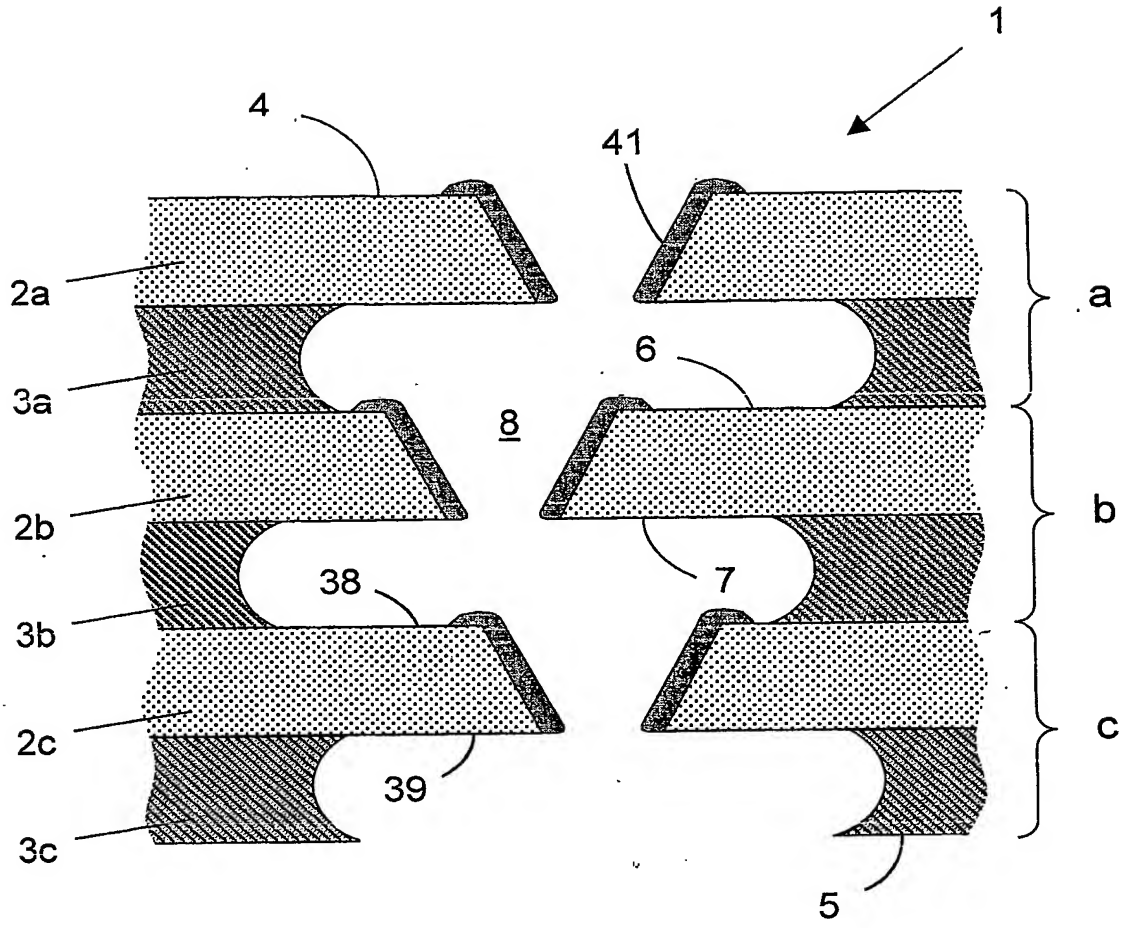


Figure 1

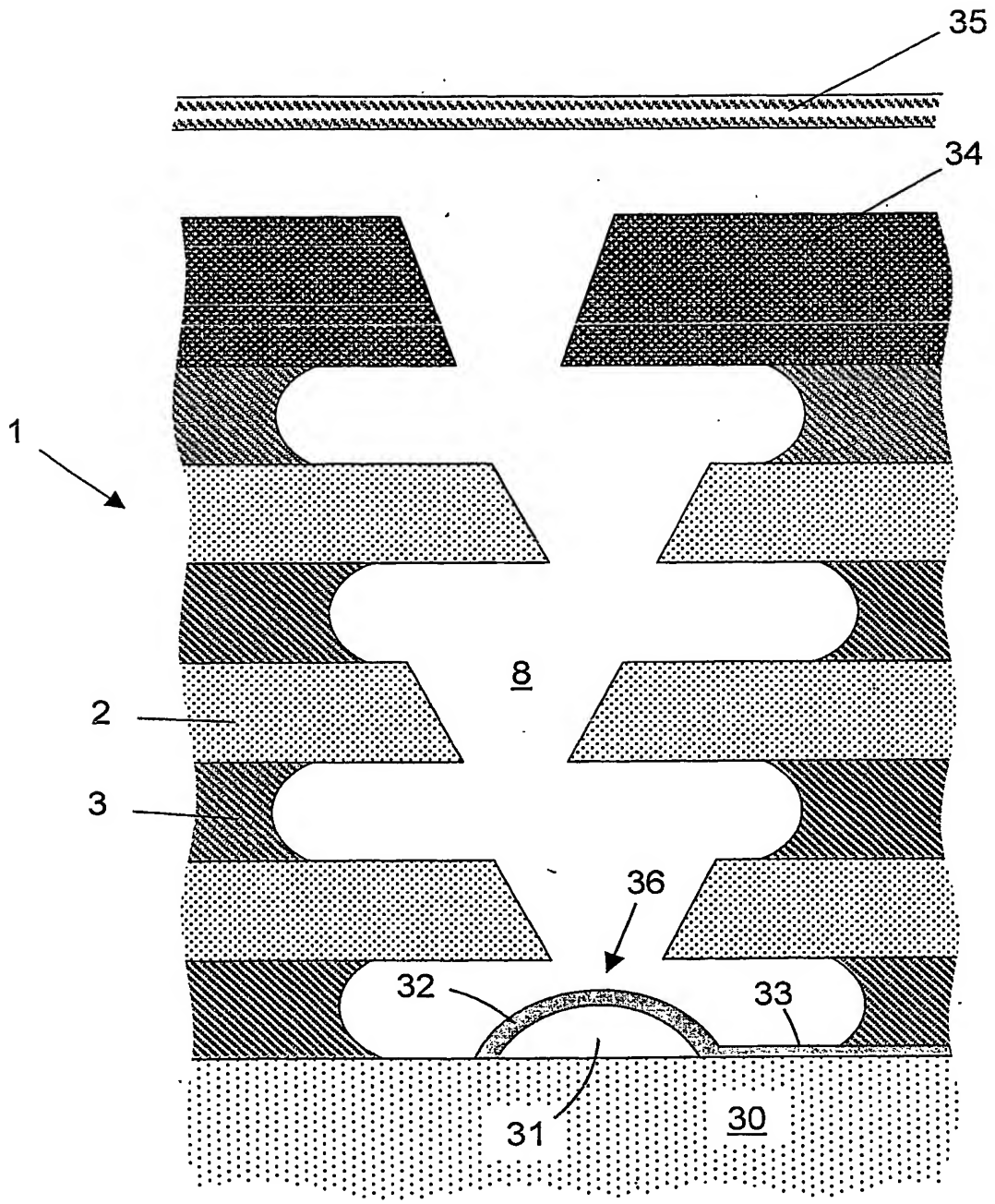


Figure 2

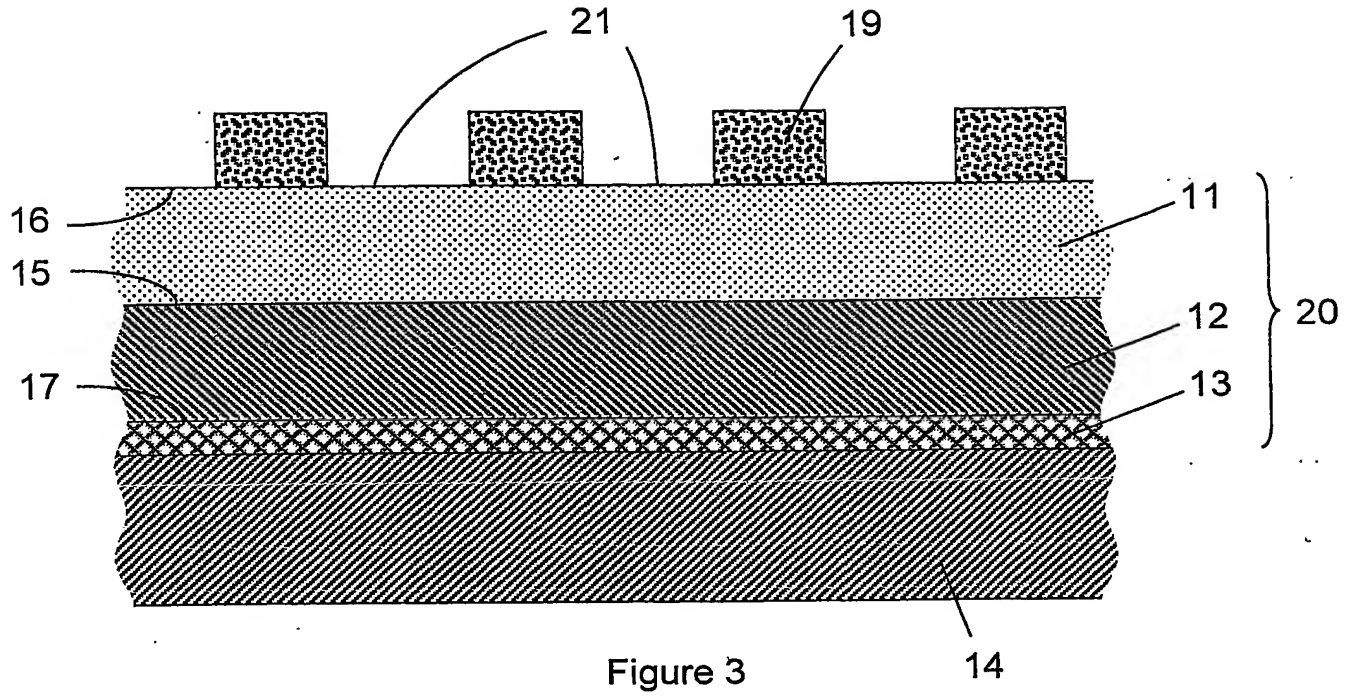


Figure 3

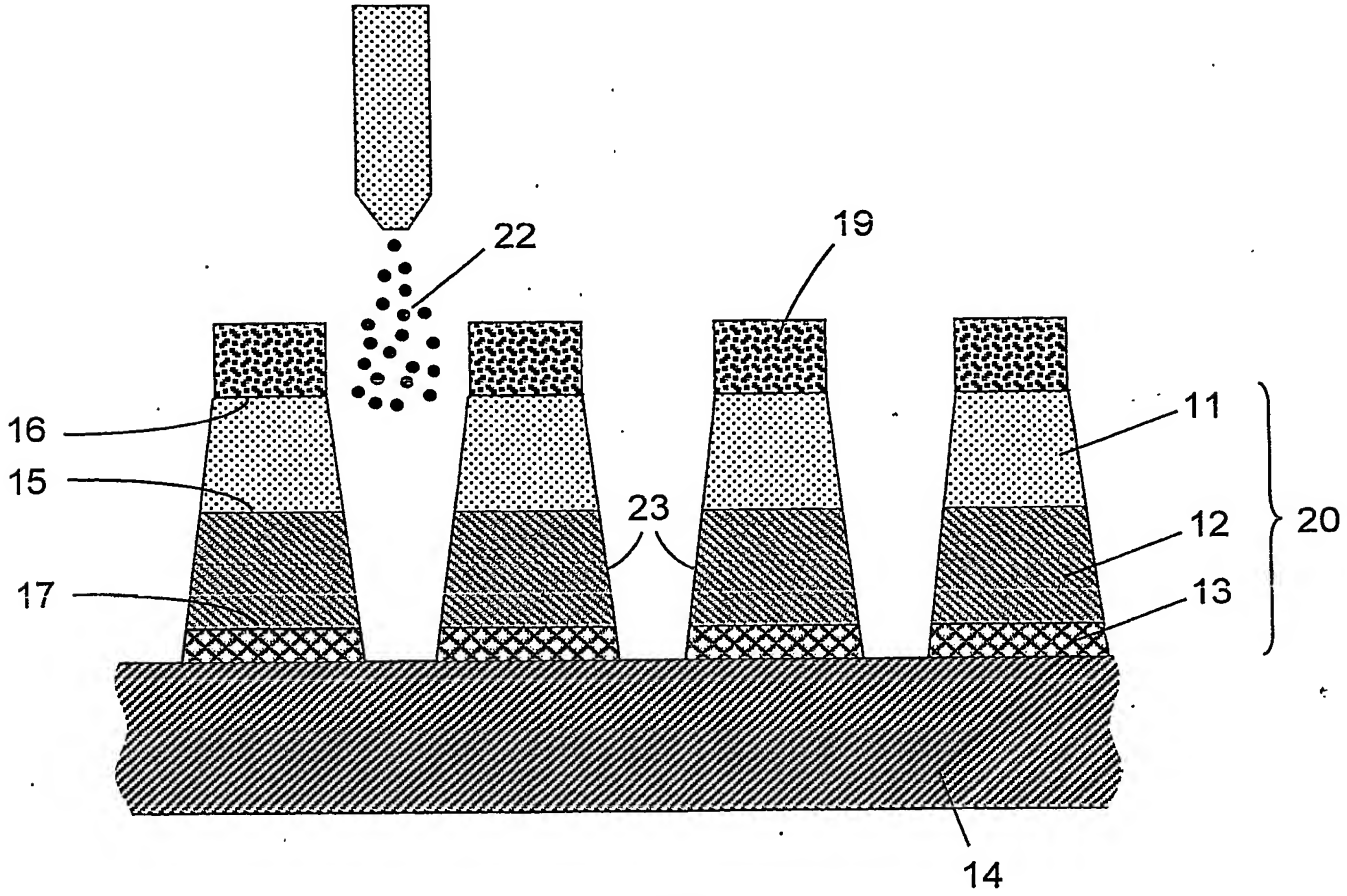


Figure 4

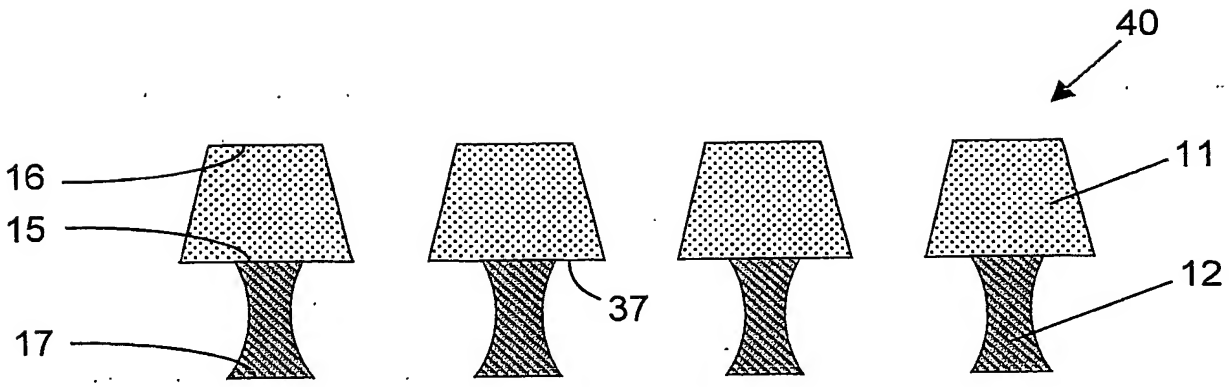


Figure 5

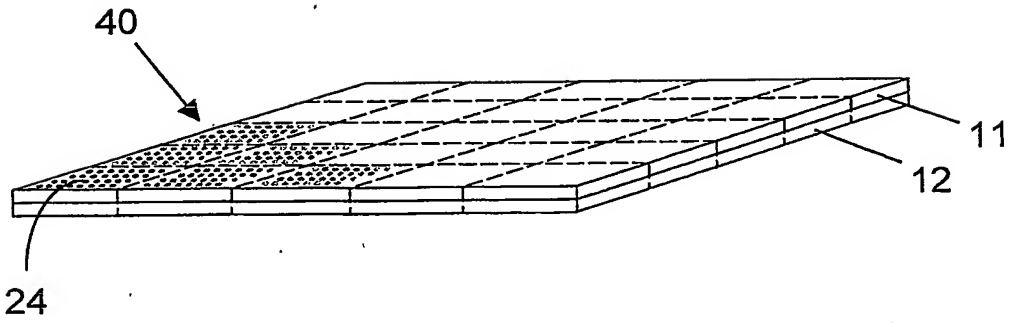


Figure 6